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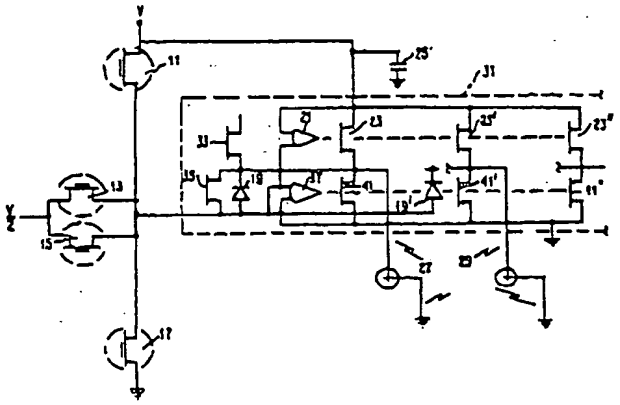
(54) Plasma display devices with sustain signal generator circuits.

(57) The drive system of a plasma display device includes a background sustain generator which is divided between a discrete component analog generator circuit (11, 13, 15, 17) and an integrated distribution chip (31). The integrated driver chip includes Low impedance switch pairs (23, 41) controlled by a pair of comparators (21, 37) which prevent the sustain signal from being degraded during discharge of the panel. By partitioning the elements of the sustain signal generator between discrete and integrated elements, optimum integration cost, circuit performance and system reliability are achieved.



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The present invention seeks by modifying the generator circuit, to enable attainment of a reliable circuit package and provides a plasma display device in which a background sustain signal is applied to groups of conductors by a common circuit generating and distributing a sustain signal having positive and negative excursions from a reference level characterized in that the conductors are individually periodically clamped by controllable low impedence paths in the common circuit to sources at the positive or negative excursion levels, means monitoring the generated sustain signal level being provided to enable the appropriate sense of low impedence path when the node is within a differential threshold of either of the excursion limits.

As heretofore noted, the plasma display panel requires a high power transition drive circuit to charge and discharge what is essentially a capacitive load which is minimized if the panel lines are driven through the voltage transitions simultaneously, eliminating the impact of interactive capacitances. Upon completion of these voltage transitions, the plasma discharges, and very high currents are required to satisfy the transfer of wall charge necessary for panel operation. The panel is then driven in the opposite direction via a controlled transition to produce an AC waveform which may have a nominal value of 200 volts peak-to-peak, with a high current plasma discharge occurring at the opposite peak voltages. Such controlled voltage transitions require analog high power switching circuits, while the plasma discharges require low impedance, low power digital switches between the panel lines and the high voltage bulk power supply.

While creating the entire sustain waveform with a discrete background analog circuit would satisfy the high power transition requirements, the accumulative impedance from the background devices and distribution would not satisfy the low impedance discharge criteria. Creating the entire waveform with fully integrated drive circuits, on the other hand, would satisfy the low impedance plasma discharge requirements, but would also incorporate the high stress,

The present invention will be described further by way of example with reference to a preferred embodiment of the invention as illustrated in the accompanying drawing in which:

Fig. 1 illustrates in schematic form the combined analog and digital circuits utilized to generate the sustain signal.

Fig. 2 illustrates a waveform of the composite sustain signal generated by the preferred embodiment of the instant invention.

Referring now to the drawings and more particularly to Fig. 1 thereof, the background analog sustain signal generating circuit is indicated as comprising discrete power transistors 11, 13, 15 and 17 and the distribution sections comprises a block 31 of an integrated chip which also provides other functions (not shown). The distribution section has a V rail and an earth rail and supplies the sustain signal to a group of conductors 27, 29 from the joins of respective pairs of transistors 23, 41; 23', 41', strung between the rails. The joins are also connected to the background generator via diodes 19, 19' and a transistor 35 and to other circuits via transistor 33. A voltage comparator 21 is connected between the V rail and the generator to enable transistors 23, 23' and a voltage comprator 37 is connected between the ground rail and the generator to enable transistors 41, 41'. The operation of the arrangement will be described in terms of the timing and waveform configurations of Fig. 2. Transistor 11 is turned on at time t_1, initiating the positive controlled voltage transistion pull-up of all panel lines via associated diodes 19 to the positive level V. Normally, discharge of the panel lines occurs at time t_3, causing a high voltage negative spike to be generated which would distort the sustain waveform and substantially reduce the panel operating margin. Such a drop in the background sustain circuit is prevented by switching the driver circuits 23 into a low impedance mode to reduce the voltage spike to a nominal tolerable notch. At time t_2, voltage comparator circuit 21 senses that the transition from the reference to the upper sustain level is at or near completion, and switches on all integrated circuit devices

the high voltage level for positive transitions and 15 volts above the ground reference for negative transitions for the particular kinds of components and operating conditions presently considered though these values are given solely as an illustration. The elimination of the spike in the sustain waveform maintains the normal operating margin and permits implementation of the background circuitry in low cost discrete form. The addition of two digital comparators integrated into the driver chip adds substantially no extra cost, while improving performance as heretofore described.

By partitioning the elements of the sustain waveform between the integrated driver chip and a discrete background analog circuit, optimum integration costs, circuit performance and system reliability are achieved. The high power controlled voltage transistions are achieved via the inexpensive discrete background devices 11, 13, 15 and 17 which control all panel lines, while the low impedance, low power plasma discharge function is achieved via low stress integrated circuit modules with a pair of switches 23 and 41 for each panel line. Additionally, the partitioned analog circuits have lower performance criteria and thus are less expensive than a single circuit trying to perform all the required functions. Use of the comparator circuits provides lowest achievable stress level of the integrated output device.

There has been disclosed a composite drive system for a plasma display device having a plurality of cells defined by the intersection of orthogonal conductor arrays, the discharge of selected cells providing a visual display, comprising in combination, analog circuit means for generating a background sustain signal, said analog circuit means comprising a plurality of high voltage circuit means for generating a signal having positive and negative excusions from a reference level, a plurality of individual line driver circuits for applying said background sustain signal to the individual lines of said panel, and means for controlling the operation of said line driver circuits during

CLAIMS

1. A plasma display device in which a background sustain signal is applied to groups of conductors (27, 29) by a common circuit (see Fig. 1) generating and distributing a sustain signal having positive and negative excursions from a reference level (see Fig. 2) characterized in that the conductors are individually periodically clamped by controllable low impedence paths (23, 23'; 41, 41') in the common circuit to sources at the positive or negative excursion levels, means (21, 37) monitoring the generated sustain signal level being provided to enable the appropriate sense of low impedence path when the node is within a differential threshold of either of the excursion limits.

2. A device as claimed in claim 1 wherein the sustain signal is generated by discrete high voltage components (11, 13, 15, 17) and distributed monitored and periodically clamped by integrated low voltage components (in 31).

3. A device as claimed in claim 2 wherein the low voltage components are integrated within a chip (31) having opposite polarity rails between which are strung serial pairs of integrated high/low impedance path devices (23, 41; 23', 41'), a conductor being connected to the join of each pair of devices, and to an output node of the sustain signal generator, the monitoring means comprising a pair of complementary voltage comparators (21, 37) similarly connected across the rails and to the output node and each switching the high/low impedence devices (23, 23'; 41, 41') connected to the associated rail.

4. A device as claimed in claim 3 wherein the conductor/node connection includes a switchable isolating device (35) and an alternative control device (33) for writing and erazing control.

5. A device as claimed in claim 4 wherein diodes (19) are connected, in the same sense, in parallel with the switchable isolating device, to each conductor.

FIG. 1

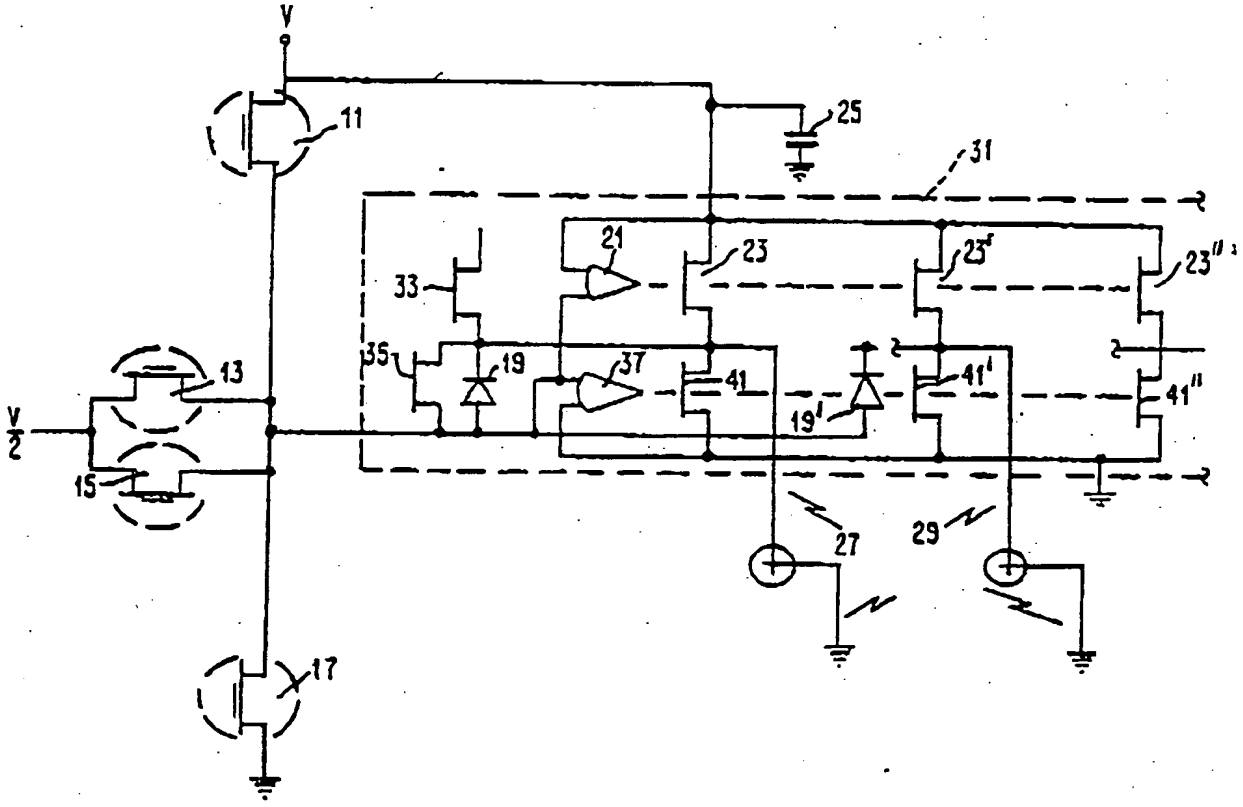
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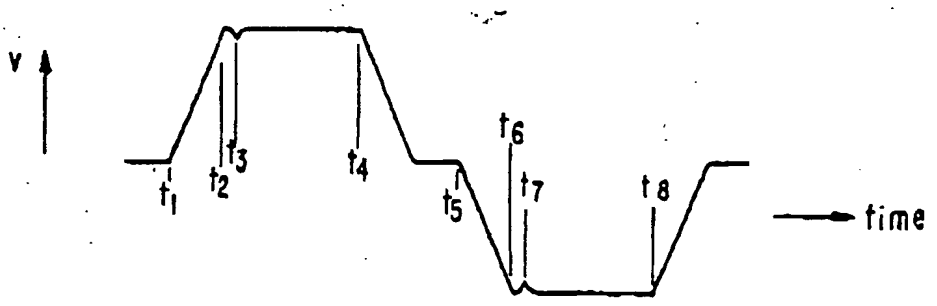
FIG. 2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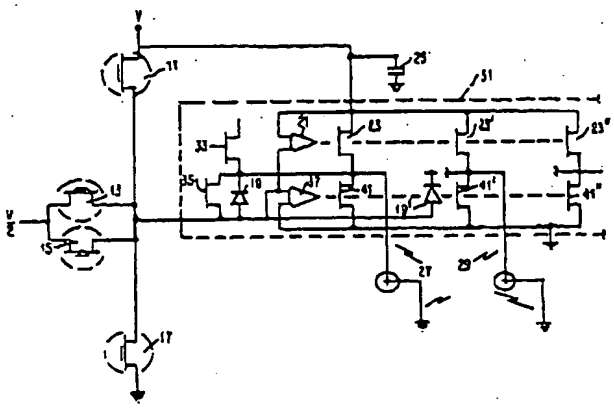

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PLASMA DISPLAY DEVICES WITH SUSTAIN SIGNAL GENERATOR CIRCUITS

In plasma display devices, conductor arrays disposed on glass substrates are overcoated with a dielectric layer, and the glass plates sealed with the conductor arrays disposed orthogonal to each other, the conductor intersections defining display cells. By applying suitable drive signals selectively to the conductor arrays, the cells located at the intersection of the conductors are discharged, creating a visible display. The resulting wall charge, which occurs on the dielectric surface adjacent the cell area after discharge, produces a wall charge potential which opposes the discharge potential and combines with a sustain signal applied to all conductors to turn off the cells shortly after discharge and to discharge the cells on the next sustain iteration.

Heretofore, see for example EP 32196, the sustain signal is provided by a background circuit which is generally a high speed, high current, high voltage, low impedance device. The sustain signal is applied through a series of individual driver circuits to all lines of the panel, where it may be combined with a write or erase signal on a selected basis. From a technology and cost standpoint, it is desirable to package the drive circuitry and other electronics in integrated circuit packages or chips. Since all discharges in the display occur simultaneously, and since the device represents a capacitive load which is continuously charged and discharged, the circuit specifications for such devices are demanding. Integrated circuits are ideally suited for high density, low voltage, low power digital signal processing and integrating such parameters into an integrated circuit chip will produce the lowest cost and size for a given function. However, the specifications for high voltage, high current drivers or switching circuits in integrated circuits are extremely demanding and the devices, if available, are extremely expensive. Thus, the panel drive waveforms are generated by a combination of analog and digital components and of high power and low power segments which are normally incompatible, particularly for high density packaging in integrated or semiconductor technology.

The present invention seeks by modifying the generator circuit, to enable attainment of a reliable circuit package and provides a plasma display device in which a background sustain signal is applied to groups of conductors by a common circuit generating and distributing a sustain signal having positive and negative excursions from a reference level characterized in that the conductors are individually periodically clamped by controllable low impedence paths in the common circuit to sources at the positive or negative excursion levels, means monitoring the generated sustain signal level being provided to enable the appropriate sense of low impedence path when the node is within a differential threshold of either of the excursion limits.

As heretofore noted, the plasma display panel requires a high power transition drive circuit to charge and discharge what is essentially a capacitive load which is minimized if the panel lines are driven through the voltage transitions simultaneously, eliminating the impact of interactive capacitances. Upon completion of these voltage transitions, the plasma discharges, and very high currents are required to satisfy the transfer of wall charge necessary for panel operation. The panel is then driven in the opposite direction via a controlled transition to produce an AC waveform which may have a nominal value of 200 volts peak-to-peak, with a high current plasma discharge occurring at the opposite peak voltages. Such controlled voltage transitions require analog high power switching circuits, while the plasma discharges require low impedance, low power digital switches between the panel lines and the high voltage bulk power supply.

While creating the entire sustain waveform with a discrete background analog circuit would satisfy the high power transition requirements, the accumulative impedance from the background devices and distribution would not satisfy the low impedance discharge criteria. Creating the entire waveform with fully integrated drive circuits, on the other hand, would satisfy the low impedance plasma discharge requirements, but would also incorporate the high stress,

high power analog switching requirements which would affect the density, yield and reliability capabilities of the integrated circuit.

It is proposed to implement analog and digital circuits in a partitioned drive system in which each circuit type can provide its optimum function. The available result is a single, inexpensive background analog circuit using discrete components which provides DC voltage transitions to the capacitive panel lines and dissipates the accompanying switching power, and an integrated driver pair for each panel line which are switched on after the voltage transitions to provide a discharge path for the plasma discharge currents. Since the plasma discharge is very rapid and of short duration, the integrated circuit devices would be low current devices with AC capability which would occupy low chip area and allow for high density packaging. The integrated devices must be capable of tolerating, say 100 to 200 volts, but are switched at less than, say, 15 volts, so high stress conditions are avoided. The resultant increased chip yields from low voltage switching circuits would provide the lowest possible integrated circuit costs. Additionally, since the background analog circuit handles the DC level shifting, the component count for the integrated circuit is optimized.

In other words there is proposed a technique of partitioning plasma discharge display panels drive circuitry to optimize the advantages of maximum integration and thereby provide the lowest cost, highest performance, and most reliable system operation by using a technique for reducing high stress conditions on integrated output drivers via voltage comparator gates which allow the device to switch only when there is negligible voltage across the device. This provides improved system performance and operating margins, while avoiding the disadvantages of alternative circuit topologies while optimizing the drive circuits with significant system cost and size reduction.

The present invention will be described further by way of example with reference to a preferred embodiment of the invention as illustrated in the accompanying drawing in which:

Fig. 1 illustrates in schematic form the combined analog and digital circuits utilized to generate the sustain signal.

Fig. 2 illustrates a waveform of the composite sustain signal generated by the preferred embodiment of the instant invention.

Referring now to the drawings and more particularly to Fig. 1 thereof, the background analog sustain signal generating circuit is indicated as comprising discrete power transistors 11, 13, 15 and 17 and the distribution sections comprises a block 31 of an integrated chip which also provides other functions (not shown). The distribution section has a V rail and an earth rail and supplies the sustain signal to a group of conductors 27, 29 from the joins of respective pairs of transistors 23, 41; 23', 41', strung between the rails. The joins are also connected to the background generator via diodes 19, 19' and a transistor 35 and to other circuits via transistor 33. A voltage comparator 21 is connected between the V rail and the generator to enable transistors 23, 23' and a voltage comprator 37 is connected between the ground rail and the generator to enable transistors 41, 41'. The operation of the arrangement will be described in terms of the timing and waveform configurations of Fig. 2. Transistor 11 is turned on at time t_1, initiating the positive controlled voltage transistion pull-up of all panel lines via associated diodes 19 to the positive level V. Normally, discharge of the panel lines occurs at time t_3, causing a high voltage negative spike to be generated which would distort the sustain waveform and substantially reduce the panel operating margin. Such a drop in the background sustain circuit is prevented by switching the driver circuits 23 into a low impedance mode to reduce the voltage spike to a nominal tolerable notch. At time t_2, voltage comparator circuit 21 senses that the transition from the reference to the upper sustain level is at or near completion, and switches on all integrated circuit devices

23, 23', 23''. When the plasma discharge occurs at time t_3, a low impedance current path is provided from the high voltage capacitor 25 to the panel lines 27, 29 via devices 23, 23', etc. While the driver integrated circuits shown as block 31 illustrates only two individual drive circuits, it will be understood that in practice a plurality of such drivers, 32 in the preferred embodiment, would be packaged in a single integrated circuit chip for optimal circuit density. The operation is completed by turning transistors 11 and 23 off prior to time t_4.

At time t_4, transistor switch 13 is turned on to pull the panel capacitance down to the reference level via device 35 to ease the stress conditions for switch 17. For purposes of this description, the stress condition defines a condition where a heavy power load instantaneously applied to a chip may self-destruct the chip. Discrete device 17 is turned on at time t_5, pulling the panel lines from the reference level to the negative transition level via device 35. Voltage comparator circuit 37 senses completion of the negative voltage transition and switches on all integrated devices 41, 41', etc. A second plasma discharge occurs at time t_7 via the low impedance path of switches 41. Prior to time t_8, devices 17 and 41 are turned off and at time t8, discrete device 15 pulls the panel lines back to the reference level and the cycle is repeated. The analog circuit configuration indicates how 100 volt circuits are used to generate a 200 volt peak-to-peak sustain signal using discrete transistors. Since the level switching represents a simple operation for a power switching device, low cost, high tolerance circuits may be utilized without any degradation in system performance.

Complementary devices 33 and 35, which form part of the integrated circuit package, provide the selection of panel lines during write and erase conditions. During normal sustain, device 35 is always on and device 33 always off. Voltage comparators 21, 37 are integrated into circuit chip 31, and sense a voltage level approximately 15 volts below

the high voltage level for positive transitions and 15 volts above the ground reference for negative transitions for the particular kinds of components and operating conditions presently considered though these values are given solely as an illustration. The elimination of the spike in the sustain waveform maintains the normal operating margin and permits implementation of the background circuitry in low cost discrete form. The addition of two digital comparators integrated into the driver chip adds substantially no extra cost, while improving performance as heretofore described.

By partitioning the elements of the sustain waveform between the integrated driver chip and a discrete background analog circuit, optimum integration costs, circuit performance and system reliability are achieved. The high power controlled voltage transistions are achieved via the inexpensive discrete background devices 11, 13, 15 and 17 which control all panel lines, while the low impedance, low power plasma discharge function is achieved via low stress integrated circuit modules with a pair of switches 23 and 41 for each panel line. Additionally, the partitioned analog circuits have lower performance criteria and thus are less expensive than a single circuit trying to perform all the required functions. Use of the comparator circuits provides lowest achievable stress level of the integrated output device.

There has been disclosed a composite drive system for a plasma display device having a plurality of cells defined by the intersection of orthogonal conductor arrays, the discharge of selected cells providing a visual display, comprising in combination, analog circuit means for generating a background sustain signal, said analog circuit means comprising a plurality of high voltage circuit means for generating a signal having positive and negative excusions from a reference level, a plurality of individual line driver circuits for applying said background sustain signal to the individual lines of said panel, and means for controlling the operation of said line driver circuits during

discharge of said selected cells to compensate for the degradation of said background sustain signal due to said discharge.

The plurality of high voltage circuit means in said analog circuits may comprise a plurality of high voltage switching means for switching high voltage levels from said reference level and the high voltage switching means include a plurality of discrete switching devices.

The individual line driver circuits may comprise an integrated driver pair for each of said panel lines to provide a discharge path for each of said selected cells.

The means for controlling the operation of said line driver circuits during discharge may comprise means for generating a signal to maintain said background circuit at its prescribed level during discharge of said selected cells.

The signal generating means may comprise voltage comparator circuits associated with said line drivers.

The voltage comparator circuits may have said high voltage switching means as one of its outputs.

The individual line drivers, driver pair, and voltage comparator circuits may be implemented in integrated circuit technology, together with means for selectively generating write or erase signals.

CLAIMS

1. A plasma display device in which a background sustain signal is applied to groups of conductors (27, 29) by a common circuit (see Fig. 1) generating and distributing a sustain signal having positive and negative excursions from a reference level (see Fig. 2) characterized in that the conductors are individually periodically clamped by controllable low impedence paths (23, 23'; 41, 41') in the common circuit to sources at the positive or negative excursion levels, means (21, 37) monitoring the generated sustain signal level being provided to enable the appropriate sense of low impedence path when the node is within a differential threshold of either of the excursion limits.

2. A device as claimed in claim 1 wherein the sustain signal is generated by discrete high voltage components (11, 13, 15, 17) and distributed monitored and periodically clamped by integrated low voltage components (in 31).

3. A device as claimed in claim 2 wherein the low voltage components are integrated within a chip (31) having opposite polarity rails between which are strung serial pairs of integrated high/low impedance path devices (23, 41; 23', 41'), a conductor being connected to the join of each pair of devices, and to an output node of the sustain signal generator, the monitoring means comprising a pair of complementary voltage comparators (21, 37) similarily connected across the rails and to the output node and each switching the high/low impedence devices (23, 23'; 41, 41') connected to the associated rail.

4. A device as claimed in claim 3 wherein the conductor/node connection includes a switchable isolating device (35) and an alternative control device (33) for writing and erazing control.

5. A device as claimed in claim 4 wherein diodes (19) are connected, in the same sense, in parallel with the switchable isolating device, to each conductor.

6. A device as claimed in claim 2 or any claim appendant thereto in which the sustain voltage generator comprises a serial pair of power transistors (11, 17) connected between ambient high and low voltage sources, having the connection therebetween clamped by a power transistor clamp (13, 15) to the reference level.

FIG. 1

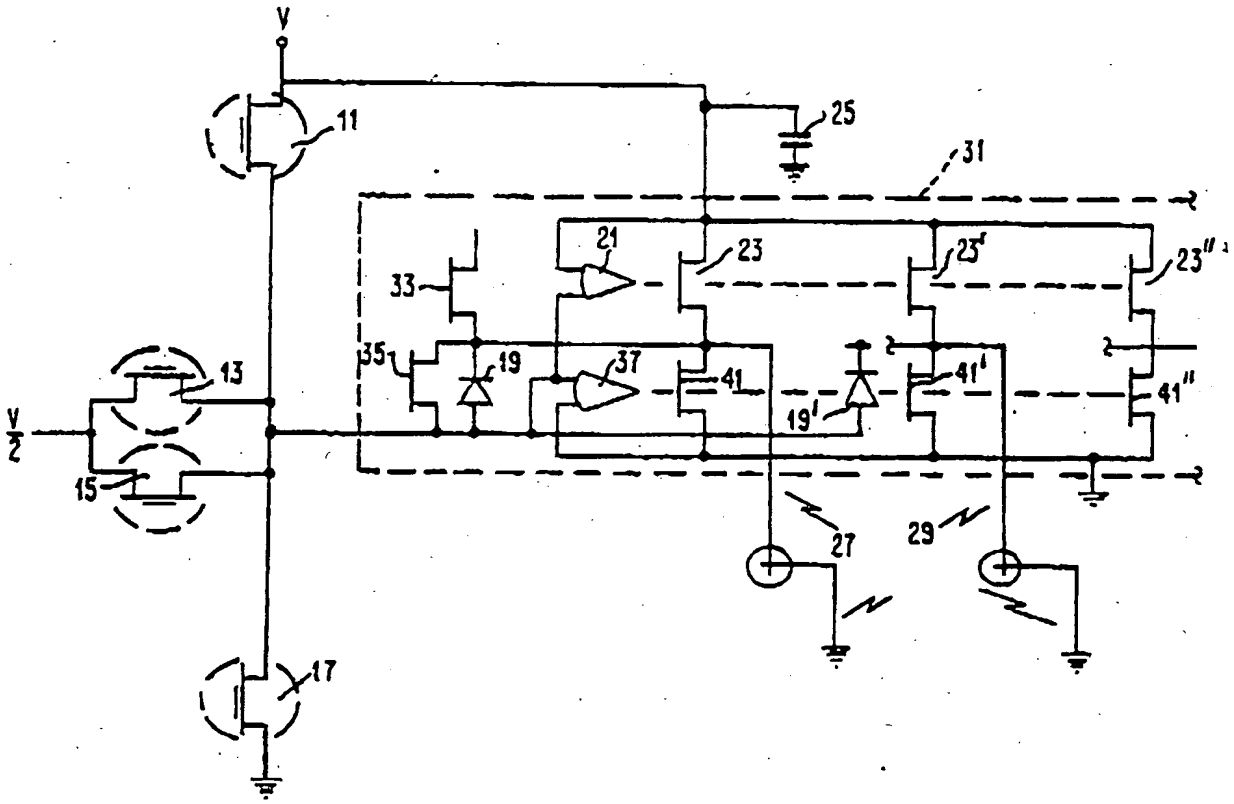
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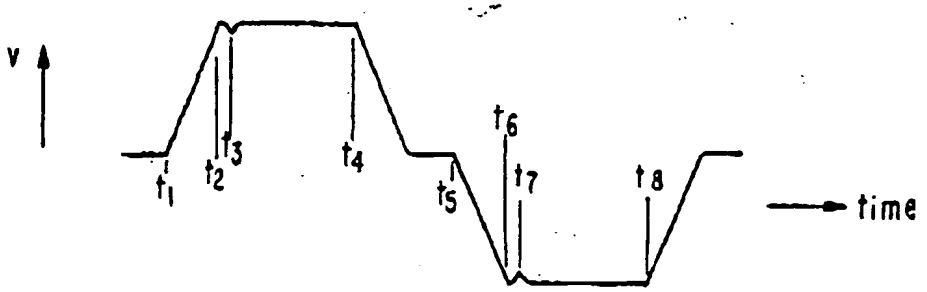
FIG. 2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